

Docket No.: P2001,0158

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : WOLFGANG GUSTIN ET AL.
Filed : CONCURRENTLY HEREWITH
Title : SEMICONDUCTOR MEMORY CELL AND METHOD FOR
FABRICATING THE MEMORY CELL

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,744,386 (Kenney), dated April 28, 1998;

U.S. Patent No. 5,827,765 (Stengl et al.), dated October 27, 1998;

U.S. Patent No. 5,670,805 (Hammerl et al.), dated September 23, 1997;

U.S. Patent No. 5,360,758 (Bronner et al.), dated November 1, 1994;

U.S. Patent No. 6,509,599 B1 (Wurster et al.), dated January 21, 2003, and
corresponding European Patent Application EP 0 971 414 A1 (Wurster et al.), dated
January 12, 2000;

German Patent DE 196 20 625 C1 (Risch et al.), dated October 23, 1997, and
English abstract thereof;

German Published Non-Prosecuted Patent Application DE 100 45 694 A1
(Schrems), dated April 4, 2002, and English translation thereof;

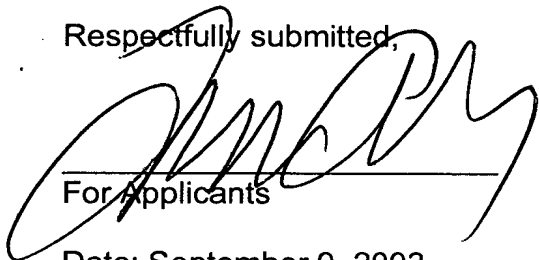
PCT WO 00/35006 (Agahi et al.), dated June 15, 2000;

Gruening, U. et al.: "A Novel DRAM Cell with a VERTICAL Access Transistor and
BuriEd STrap (VERI BEST) for 4Gb/16Gb", IEEE, 1999, 4 pages;

International Search Report, dated March 17, 2003.

If no translation of pertinent portions of any foreign language patents or publications
mentioned above is included with the aforementioned copies of those applications,
patents and/or publications, it is because no existing translation is readily available to
the applicant.

Respectfully submitted,



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For Applicants

Date: September 9, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: P2001,0158 Appl. No.: Applicant: WOLFGANG GUSTIN ET AL. Filing Date: September 9, 2003 Group Art Unit:			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	5,744,386	4/28/98	Kenney			
	B	5,827,765	10/27/98	Stengl et al.			
	C	5,670,805	9/23/97	Hammerl et al.			
	D	5,360,758	11/1/94	Bronner et al.			
	E	6,509,599 B1	1/21/03	Wurster et al.			
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J	196 20 625 C1	10/23/97	Germany			
	K	100 45 694 A1	4/4/02	Germany			
	L	0 971 414 A1	1/12/00	Europe			
	M	00/35006	6/15/00	WIPO			
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
		Gruening, U. et al.: "A Novel DRAM Cell with a VERTlcal Access Transistor and BuriEd STRap (VERI BEST) for 4Gb/16Gb", IEEE, 1999, 4 pages					
EXAMINER				DATE CONSIDERED			